UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,370	04/23/2001	Masaru Iida	010570	2325

23850 7590 02/24/2005

ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP
1725 K STREET, NW
SUITE 1000
WASHINGTON, DC 20006

EXAMINER	
PHAM, HAI CHI	

ART UNIT	PAPER NUMBER
2861	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/839,370	IIDA, MASARU	
	Examiner	Art Unit	
	Hai C. Pham	2861	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,7 and 8 is/are rejected.

7)☒ Claim(s) 2-6 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 06/19/01.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Fudeyasu (Pub. No. U.S. 2002/0023191).

Fudeyasu discloses a data sequence conversion circuit (bit-width conversion circuit) (Figs. 15-17), which takes as an input any one of a plurality of input data sequences having different data widths (M or N-bit data), and which converts said input data sequence into an output data sequence having a prescribed data width (P-bit data) for output, said circuit comprising a first parallel shift register (tri-state input buffer circuit 70) for holding said input data sequence, a switch matrix (switch matrix 72a) for taking the data held in said first parallel shift register as input data, and for outputting said input data in a distributed fashion in accordance with a rule selected by a control signal from a plurality of predetermined rules (using the write transfer control circuit 72b for generating selection signals Φ1 – Φ8), and a second parallel shift register (latch circuit 72d) for taking the data output from said switch matrix as input data, and for outputting said input data as a data sequence having said prescribed data width (P-bit data) (see discussion related to Figs. 15-17).

With regard to claim 7, Fudeyasu further teaches each time QIn data sequences are input into said first parallel shift register, Wn.times.QIn units of data are input into said second parallel shift register via said switch matrix, following which QOn data sequences are output from said second parallel shift register (the output data bus-line 13 being adapted to accommodate for the input bit-width data).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Acknowledged Prior Art (hereinafter referred as AAPA) in view of Fudeyasu.

AAPA discloses an LED printer comprising a data sequence conversion circuit (60) located between a jaggy correction circuit (50) and a line printhead (26) (Fig. 7).

However, AAPA fails to teach the first parallel shift register, the switch matrix and the second parallel shift register.

Fudeyasu discloses a data sequence conversion circuit (bit-width conversion circuit) (Figs. 15-17), which includes the first parallel shift register, the switch matrix and the second parallel shift register (see rejection in above paragraph 3).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to provide AAPA device with the first parallel shift register, the switch matrix and the second parallel shift register as taught by Shimizu. The motivation for doing so would have been to increase the printing speed of the LED printer.

6. Alternatively, claims 1 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Shimizu (JP 4-207897).

AAPA discloses an LED printer comprising a data sequence conversion circuit (60) located between a jaggy correction circuit (50) and a line printhead (26) (Fig. 7).

However, AAPA fails to teach the first parallel shift register, the switch matrix and the second parallel shift register.

Shimizu, an acknowledged prior art, discloses a data sequence conversion circuit, which comprises a first parallel shift register (shift register 12) for holding said input data sequence, a switch matrix (10) for taking the data held in said first parallel shift register as input data, and for outputting said input data in a distributed fashion to a second parallel shift register (shift register 13) for taking the data output from said switch matrix as input data, and for outputting said input data as a data sequence.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to provide AAPA device with the first parallel shift register, the switch matrix and the second parallel shift register as taught by Shimizu. The motivation for doing so would have been to increase the printing speed of the LED printer.

Allowable Subject Matter

7. Claims 2-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: the primary reason for the indication of the allowability of claims 2 and 5 is the inclusion therein, in combination as currently claimed, of the limitation "the first parallel shift register has the number of stages at least equal to the largest value of the quotients QIn (n=1, 2, 3, . . .) each obtained by dividing the least common multiple of the input data width Wn and the output data width Wo by Wn", which is not found taught by the prior art of record considered alone or in combination.

The primary reason for the indication of the allowability of claim 3 is the inclusion therein, in combination as currently claimed, of the limitation "the second parallel shift register has the number of stages at least equal to the largest value of the quotients QOn (n=1, 2, 3, . . .) each obtained by dividing the least common multiple of the input data width Wn and the output data width Wo by Wo", which is not found taught by the prior art of record considered alone or in combination.

The primary reason for the indication of the allowability of claim 4 is the inclusion therein, in combination as currently claimed, of the limitation "wherein the data widths of said plurality of input data sequences are 5 bits, 4 bits, and 3 bits, respectively, the data width of said output data sequence is 8 bits, said first

parallel shift register has a 5-bit data width and eight stages, and said second parallel shift register has five stages", which is not found taught by the prior art of record considered alone or in combination.

The primary reason for the indication of the allowability of claim 6 is the inclusion therein, in combination as currently claimed, of the limitation "wherein the shift clock frequency Fi of said first parallel shift register and the shift clock frequency Fo of said second parallel shift register have a relation defined by Fi/Fo=Wo/Wn", which is not found taught by the prior art of record considered alone or in combination.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai C. Pham whose telephone number is (571) 272-2260. The examiner can normally be reached on M-F 8:30AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (571) 272-1934. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HAI PHAM
PRIMARY EXAMINER

February 22, 2005